VLSI

Curriculum

Dream Tech Labs
A unit of DREAM WEAVERS Group
An ISO 9001:2008 Certified Company
Development | Training | Consultancy

Durations: (45 Days)

Basics of VLSI (2Days)

Introduction to VLSI
VLSI Design Flow
ASIC
SOC

Digital System Design: (13 Days)

Fundamentals of digital designs

Number Systems
Basic digital circuits
Logic Gates & Boolean Algebra
Logic families

Combination Circuits

Multiplexer
De-multiplexer
Encoder/Priority Encoder
Decoder
Adder / Subtractor / Multiplier / Divider
ALU Designing

Sequential Circuits

Bi-stable elements
Latches and Flip-flops
Synchronous & asynchronous circuits
Counters
Registers
Digital design methodology

Advance Digital Design

State Machines
Clocked synchronous state machine analysis
Clocked synchronous state machine design
Finite state machines
Mealy/Moore machines
State reduction techniques
ASM charts
Clock dividers
FIFO & pipelining
PLD/CPLD

VERILOG: (20 Days)

Overview of digital design with VERILOG HDL

Cad tools
Evolution of cad tools
Emergence of HDL's
HDL based design flow
Why VERILOG
Trends in VERILOG

Hierarchical modeling concept

Top-down and bottom up methodology
Differences between module and module instances
Parts of a simulation
Design block
Stimulus block

Basic concepts

Lexical conventions
Data types
System tasks
Compiler directives

Modules and ports

Module definition
Port declaration
Connecting ports
Port mapping

Gate-level modeling

Circuit designing using Verilog gate primitives
Description of logic gates and buf. Type gates
Rise/fall/turn off/min/max/typical delays

Dataflow modeling

Continuous assignments
Delay specifications
Expressions
Operators
Operands
Operator types

Behavioral modeling

Structured procedures
Initial and always statements
Blocking/non-blocking statements
Delay control

Event control
Conditional statements
Multi-way branching
Loops
Sequential and parallel blocks

Tasks and functions

Difference between task and functions
Declaration
Invocation
Automatic task and function

Useful modeling techniques

Procedural continuous assignments
Conditional compilation and execution
Useful system task

LIVE PROJECT (10 Days)

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